FIG. 1

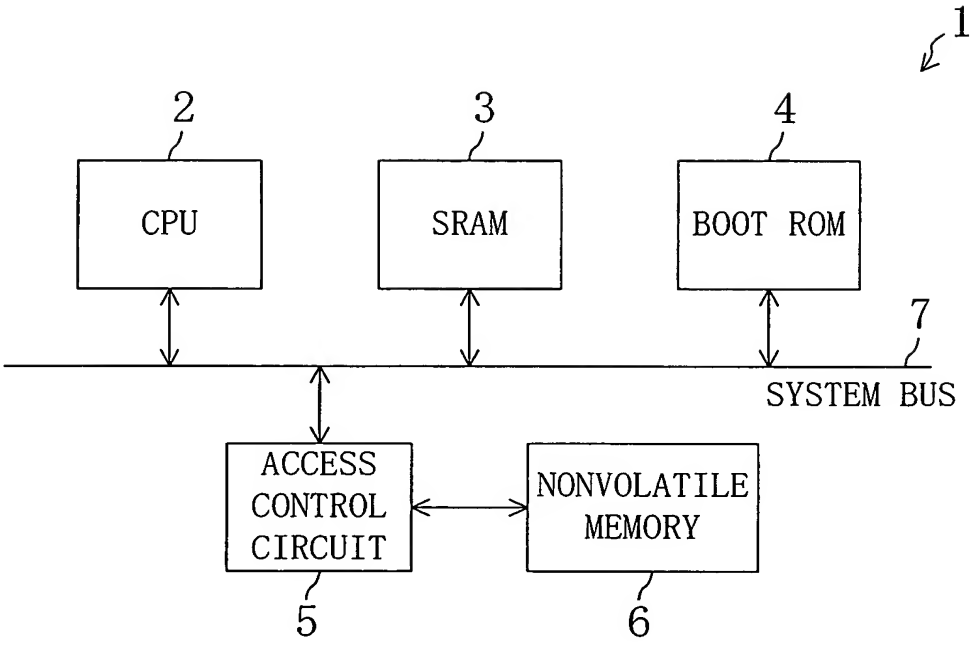

1
2
3
4
CPU
SRAM
BOOT ROM
7
SYSTEM BUS
ACCESS CONTROL CIRCUIT
NONVOLATILE MEMORY
5
6

FIG. 2

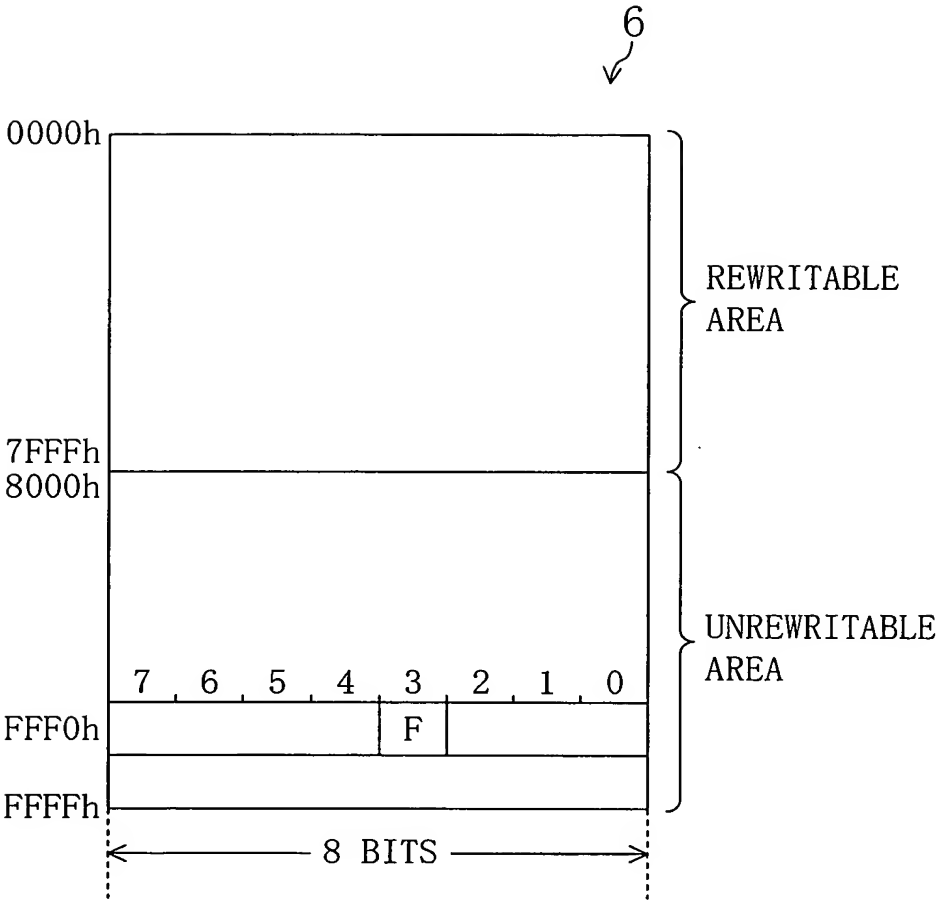

6
0000h
7FFFh
8000h
FFF0h
FFFFh
REWRITABLE AREA
UNREWRITABLE AREA
7 6 5 4 3 2 1 0
F
8 BITS

FIG. 3

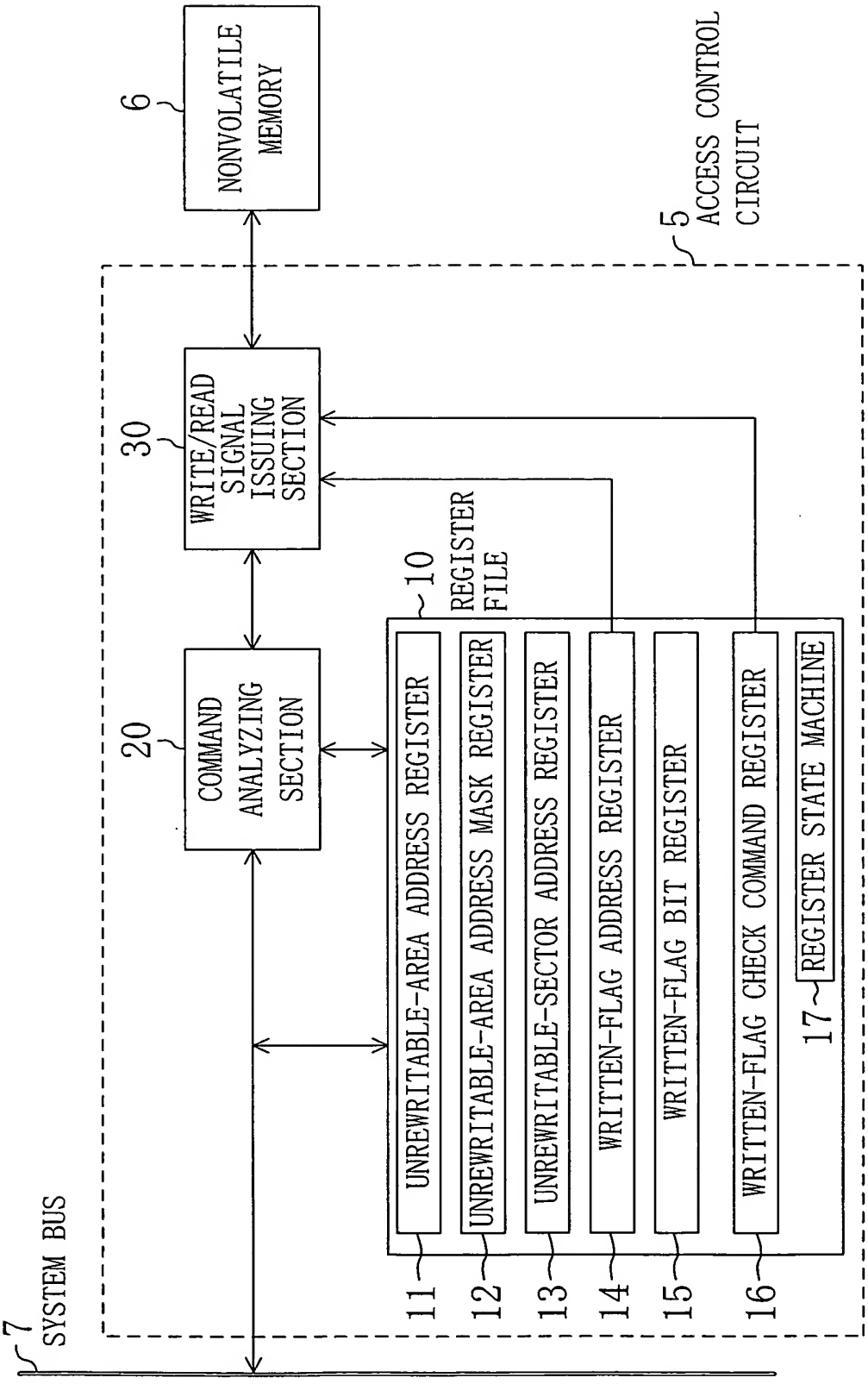

6
NONVOLATILE MEMORY
5
ACCESS CONTROL CIRCUIT
30
WRITE/READ SIGNAL ISSUING SECTION
20
COMMAND ANALYZING SECTION
10
REGISTER FILE
UNREWRITABLE-AREA ADDRESS REGISTER
UNREWRITABLE-AREA ADDRESS MASK REGISTER
UNREWRITABLE-SECTOR ADDRESS REGISTER
WRITTEN-FLAG ADDRESS REGISTER
WRITTEN-FLAG BIT REGISTER
WRITTEN-FLAG CHECK COMMAND REGISTER
REGISTER STATE MACHINE
11
12
13
14
15
16
17
7
SYSTEM BUS

FIG. 4

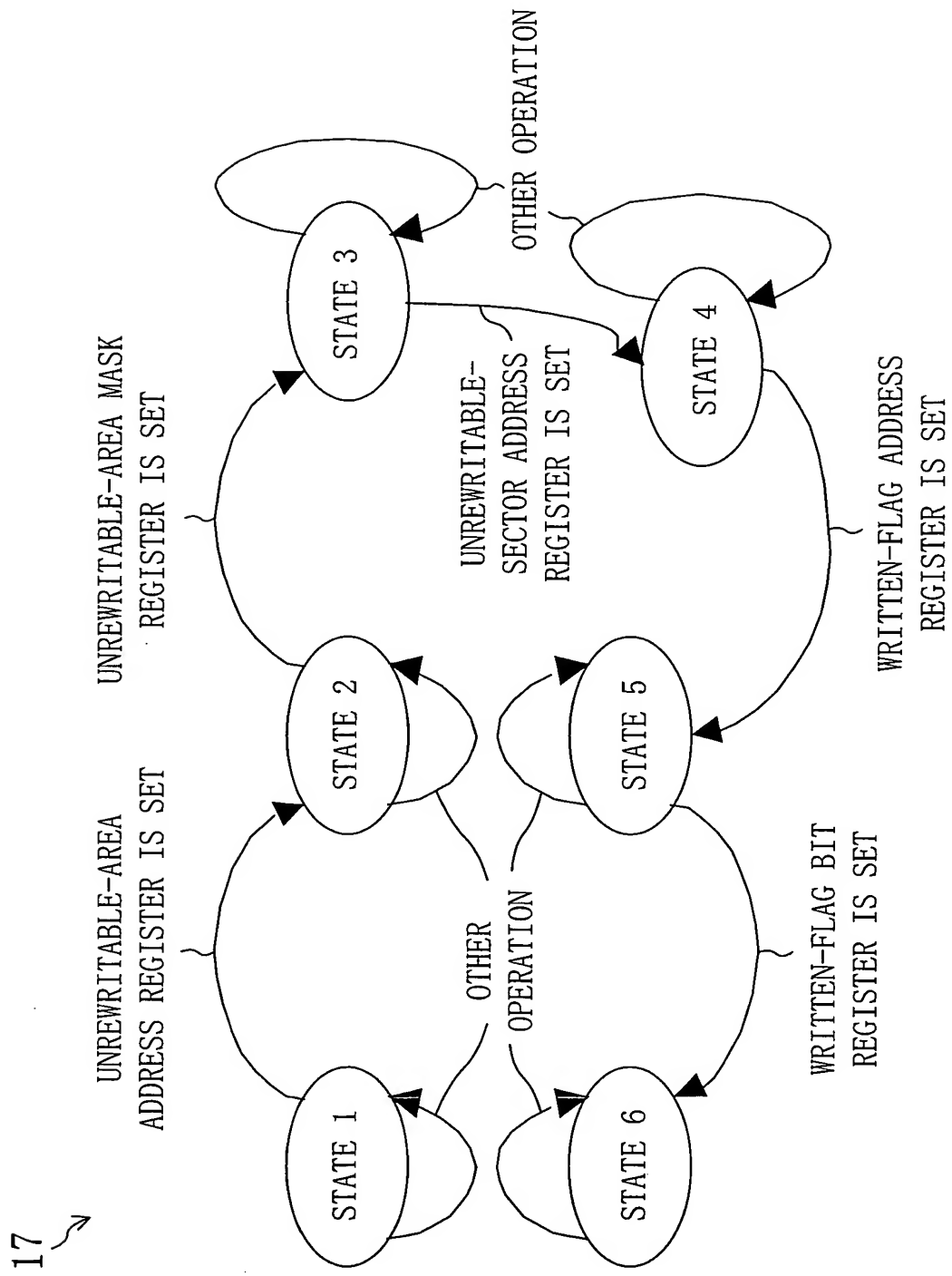

17
STATE 1
STATE 2
STATE 3
STATE 4
STATE 5
STATE 6
UNREWRITABLE-AREA ADDRESS REGISTER IS SET
UNREWRITABLE-AREA MASK REGISTER IS SET
OTHER OPERATION
UNREWRITABLE-SECTOR ADDRESS REGISTER IS SET
OTHER OPERATION
WRITTEN-FLAG BIT REGISTER IS SET
WRITTEN-FLAG ADDRESS REGISTER IS SET

FIG. 5

CYCLE		1	2	3	4	5	6
WRITE	ADRS	555h	2AAh	555h	WA	-	-
	DATA	AAh	55h	A0h	WD	-	-
SECTOR ERASE	ADRS	555h	2AAh	555h	555h	2AAh	SA
	DATA	AAh	55h	80h	AAh	55h	30h
CHIP ERASE	ADRS	555h	2AAh	555h	555h	2AAh	555h
	DATA	AAh	55h	80h	AAh	55h	10h

WA: WRITE ADDRESS
WD: WRITE DATA
SA: SECTOR ADDRESS

FIG. 6

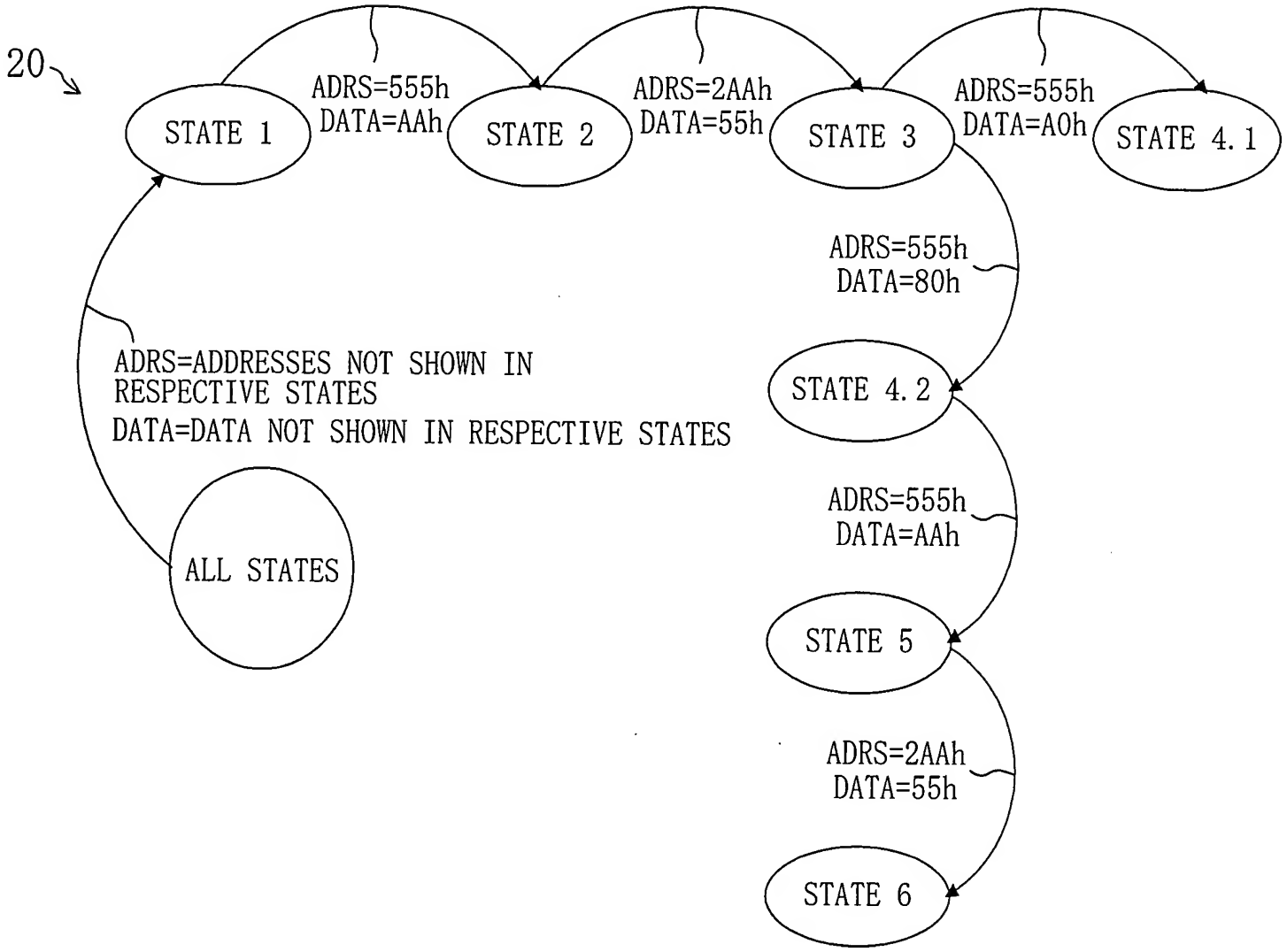

20
STATE 1
ADRS=555h
DATA=AAh
STATE 2
ADRS=2AAh
DATA=55h
STATE 3
ADRS=555h
DATA=A0h
STATE 4.1
ADRS=555h
DATA=80h
STATE 4.2
ADRS=555h
DATA=AAh
STATE 5
ADRS=2AAh
DATA=55h
STATE 6
ADRS=ADDRESSES NOT SHOWN IN RESPECTIVE STATES
DATA=DATA NOT SHOWN IN RESPECTIVE STATES
ALL STATES

FIG. 7

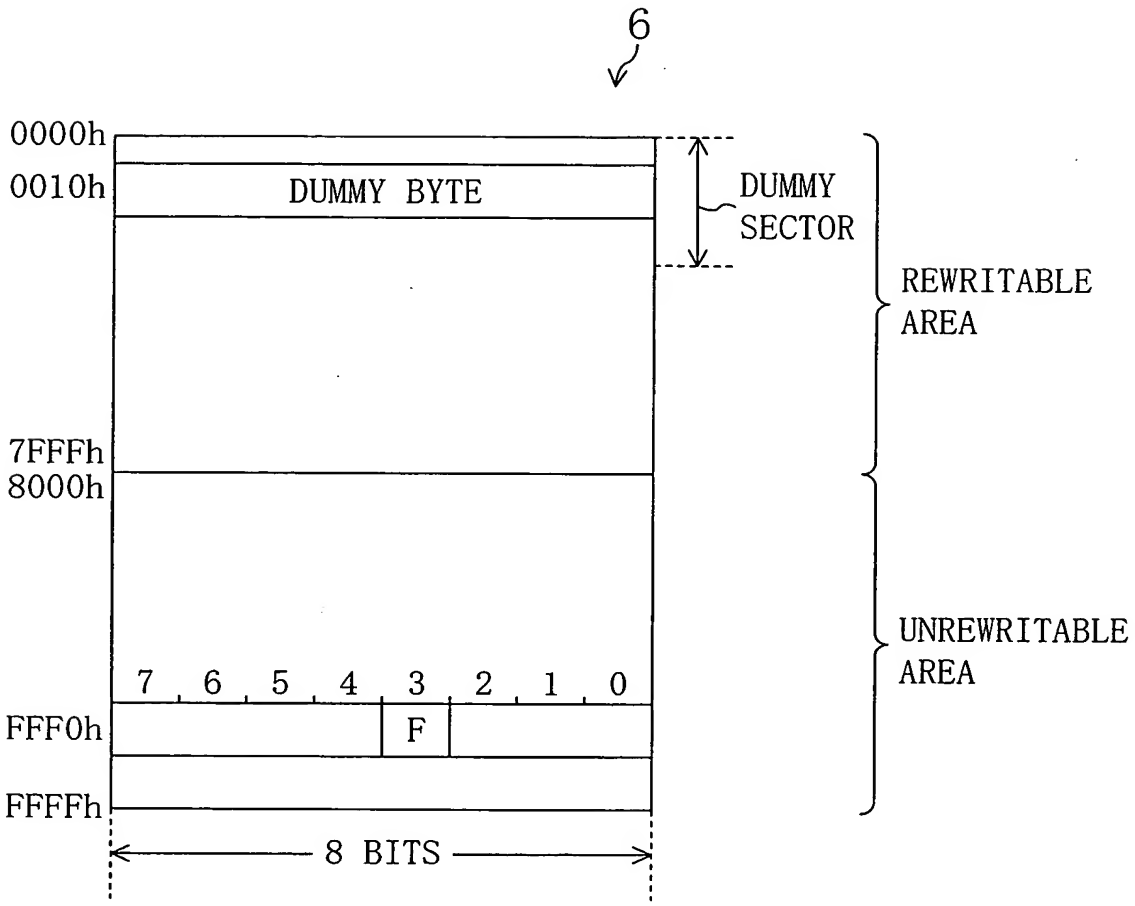

6
0000h
0010h
DUMMY BYTE
DUMMY SECTOR
REWRITABLE AREA
7FFFh
8000h
UNREWRITABLE AREA
7 6 5 4 3 2 1 0
FFF0h
F
FFFFh
8 BITS

FIG. 8

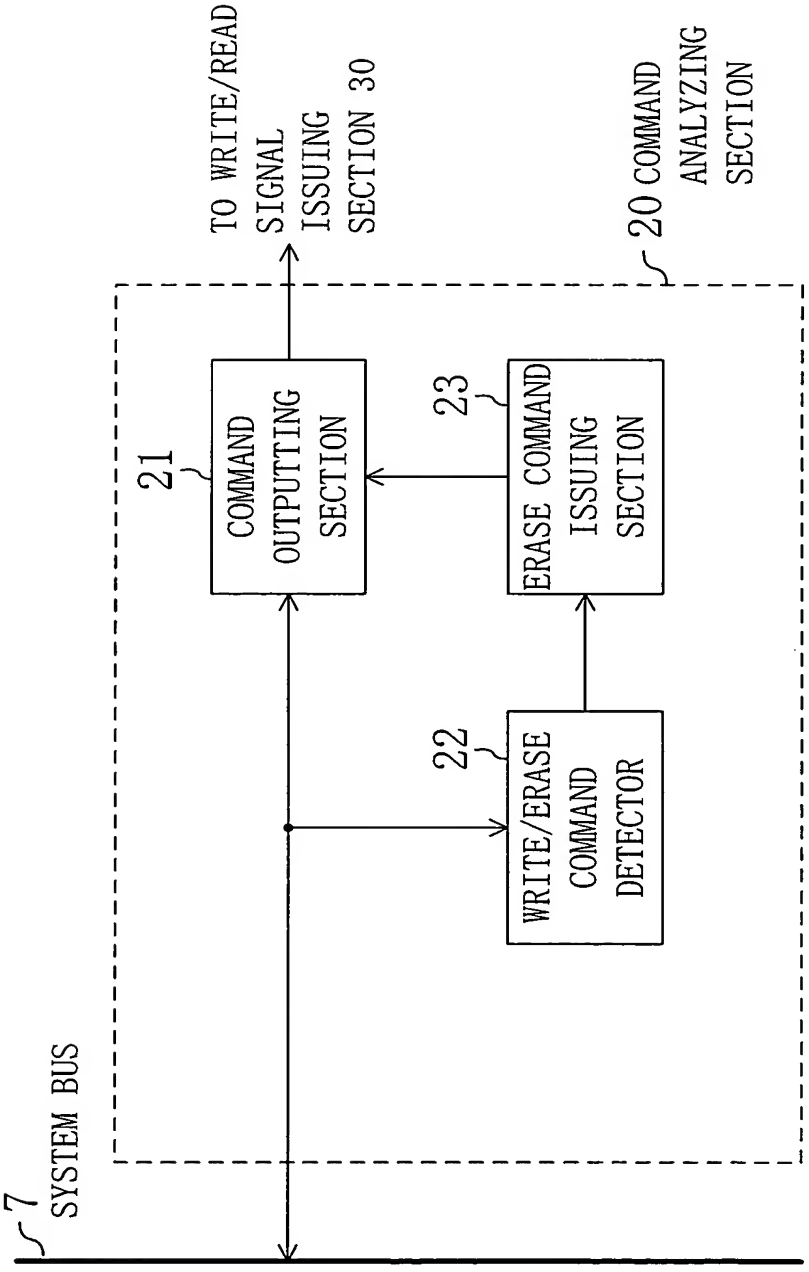
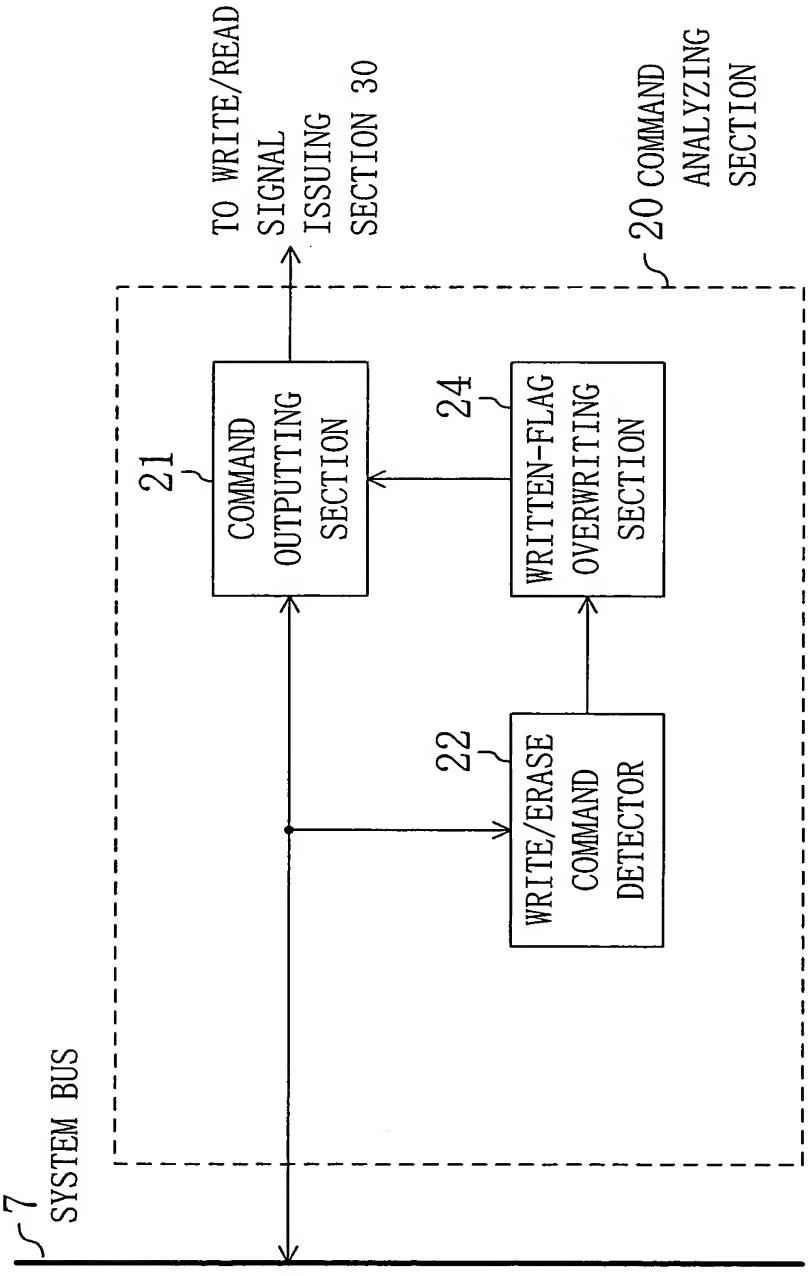

TO WRITE/READ SIGNAL ISSUING SECTION 30
20 COMMAND ANALYZING SECTION
21
COMMAND OUTPUTTING SECTION
23
ERASE COMMAND ISSUING SECTION
22
WRITE/ERASE COMMAND DETECTOR
7
SYSTEM BUS

FIG. 9


7
SYSTEM BUS
21
COMMAND OUTPUTTING SECTION
22
WRITE/ERASE COMMAND DETECTOR
24
WRITTEN-FLAG OVERWRITING SECTION
TO WRITE/READ SIGNAL ISSUING SECTION 30
20 COMMAND ANALYZING SECTION